MOSFET Qrr: Ignore at your peril in the pursuit of power efficiency

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Efficiency is often the most important factor when designing a power supply for many types of consumer and industrial applications including mobile phones, tablet and notebook computers, rechargeable power tools and LED lighting, and a myriad of other products. High efficiency may be required to meet legislative requirements, or simply to reduce the dissipated heat and thereby enable the design of smaller & lighter end products. Choosing a synchronous MOSFET to meet all of the requirements can be a bewildering task.

Naturally, engineers will look at the obvious datasheet parameters first, selecting devices with the right voltage and current ratings . Because efficiency is important most devices are primarily selected by $R_{DS(on)}$. Depending on the switching frequency, then the dynamic parameters; for example, gate charge, Q_g and Q_{gd}, can be a good indicator of the expected gate losses. The Q_g Figure Of Merit (FOM = $R_{DS(on)}$ x Q_G) is also a good indicator of a MOSFET's efficiency in a switching application, and the MOSFET's capacitance, C_{iss}, C_{oss}, C_{rss}, can predict whether drain-source spiking and gate bounce will be a problem. Low capacitance can contribute to higher efficiency also. Finally, the device must fit into your design, so you look at how big it is and what package it comes in.

However, there is another parameter, Q_{rr}, that is often ignored, and is usually found at the bottom of the datasheet. In applications where current flows through the MOSFET's body diode, for example, in a synchronous rectifier and in free-wheel applications, then the reverse recovery charge, Q_{rr}, causes some significant challenges which the design engineer needs to carefully address.

Q_{rr} or reverse recovery charge is the charge that accumulates in the PN junction of a MOSFET's body diode when the diode is forward biased. In most applications, current flows through the body diode twice for each switching cycle, causing charge to accumulate. The later dispersion of that charge, either within the MOSFET itself, or as an additional current

(I_{rr}) which flows briefly through the high-side MOSFET, and causes additional losses in the system.

A spiky character

That reverse recovery current (I_{rr}) also interacts with the PCB's parasitic inductance, to cause spikes in the drain-source voltage (VDS). These spikes can be reduced by reducing the PCB's inductance or by choosing a MOSFET with low Q_{rr}. Failure to address the spiking issue at the design stage often results in engineers having to use a higher voltage grade, and therefore more expensive MOSFET later in the project.

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But that still leaves a problem. If left untreated, then spikes at the drain pin can be capacitively-coupled to the gate pin, leading to so-called 'gate bounce'. If this gate bounce exceeds the MOSFET's threshold voltage, then cross-conduction occurs and the MOSFET can turn on when it should be off. If both the high-side and low-side MOSFETs turn on at the same time, shoot-through current occurs between the power rails causing major power losses and potentially destroying the MOSFET.

Let's look at this in more detail. Due to the dead-time needed in most applications, current flows through the body diode twice for every switching cycle. Let us first consider what happens just before the sync-fet is turned on. Since current will be flowing through the body diode during the dead-time, then some of the load current becomes trapped as stored charge, Q_{rr}.

As the sync-fet is turned on, then the stored charge is dissipated internally within the MOSFET. Therefore, a proportion of the load current is lost due to the Q_{rr} effect and contributes to I^2R loss within the sync-fet.

In the second instance, the MOSFET's body diode becomes reverse biased once again when the high-side MOSFET turns on. Additional current, I_{rr}, flows briefly through the high-side MOSFET until the stored charge, Q_{rr}, is fully depleted. The charge depletion is not instantaneous, I_{rr} typically flows for a few tens of nanoseconds until Q_{rr} is depleted. The reverse recovery time, T_{rr}, is quoted on the datasheet. In this case, then I_{rr} results in additional I^2R losses within the high-side MOSFET, as shown in **Figure 1**.

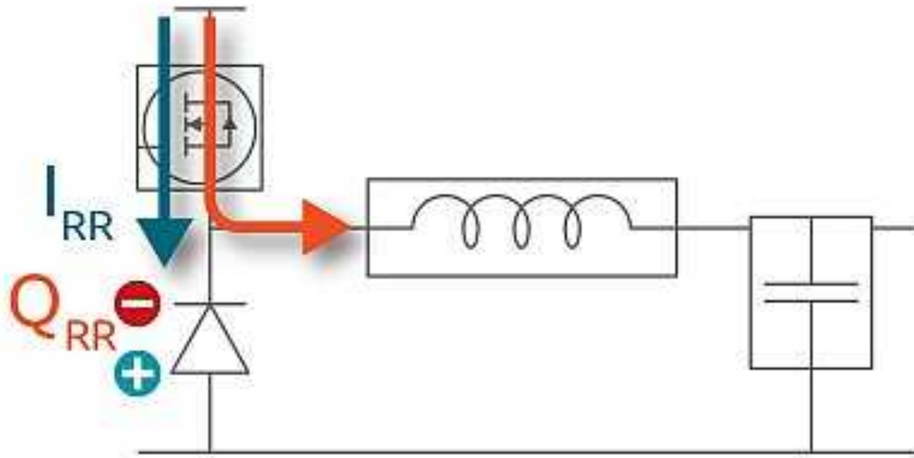

Figure 1 I_{rr} results in additional I^2R losses within the high-side MOSFET

V_{ds} spiking

Reverse recovery current spike, I_{rr}, also interacts with the PCB's parasitic inductance to create a voltage spike where:

V = L x (di/dt).

The MOSFET should be suitably rated to ensure that the breakdown voltage rating (BVDS) is higher than the maximum spike; typically an 80% derating is applied. An application with a measured 80V V_{ds} spike would typically require a MOSFET with a BVDS voltage of at least 100V.